## III. Listing of Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method of trimming a feature in a pattern formed in a photoresist layer on a substrate, comprising:

[[(a)]] providing a substrate;

[[(b)]] forming a bilayer stack comprised of a top photoresist layer and an organic underlayer on said substrate, said organic underlayer is thicker than said top photoresist layer;

[[(c)]] forming a pattern having a feature with a first width in said top photoresist layer;

[[(d)]] transferring said pattern through the organic underlayer with a first plasma etch step to produce a pattern that has a feature with a first width and sidewalls; and

[[(e)]] trimming said pattern with a second plasma etch step to give a pattern in the bilayer stack having a feature with a second width and sidewalls, said second width is smaller than said first width.

2. (Original) The method of claim 1 wherein the top photoresist layer is a silicon containing positive tone photoresist that is patterned by exposing with 193 nm, 157 nm, or EUV radiation and developing in an aqueous base solution.

3. (Original) The method of claim 1 wherein the organic underlayer has a thickness of about 1000 to 10000 Angstroms and does not react with the top photoresist layer during the photoresist coating and patterning steps.

4. (Original) The method of claim 1 wherein said first width in said top photoresist layer is less than 100 nm.

5. (Original) The method of claim 1 wherein the first plasma etch step comprises the following conditions: a 10 to 500 standard cubic centimeter per minute (sccm) flow rate of H2; a 10 to 500 sccm flow rate of N2; a 10 to 500 sccm flow rate of SO2; a chamber temperature of about 0° C to 100° C; a RF power from about 100 to 1000 Watts; and a chamber pressure between about 3 and 500 mTorr.

6. (Original) The method of claim 1 wherein the second plasma etch step comprises the following conditions: a 10 to 500 sccm Cl2 flow rate; a 1 to 50 sccm O2 flow rate; a 10 to 50 sccm HBr flow rate; a chamber temperature of about 0° C to 100° C; a RF power from about 100 to 1000 Watts; and a chamber pressure between about 3 and 500 mTorr for a period of about 5 to 200 seconds.

7. (Original) The method of claim 1 wherein the first and second plasma etch steps are performed in the same process chamber.

8. (Original) The method of claim 1 wherein the second width is more than about 10 nm smaller than the first width.

9. (Original) The method of claim 1 further comprised of transferring the pattern into said substrate with a third plasma etch step in the same process chamber as used for the second plasma etch step.

10. (Original) The method of claim 1 wherein the sidewalls formed on the organic underlayer portion of said feature are vertical or have a retrograde profile.

11. (Currently Amended) A method of forming a gate electrode in a MOSFET, comprising:

[[(a)]] providing a substrate with isolation regions formed therein and with a gate stack comprised of a gate layer on a gate dielectric layer formed on said substrate between said isolation regions;

[[(b)]] forming a bilayer stack comprised of a top photoresist layer and an organic underlayer on said gate layer, said organic underlayer is thicker than said top photoresist layer;

[[(c)]] forming a pattern having a feature with a first width in said top photoresist layer;

[[(d)]] transferring said pattern through the organic underlayer with a first plasma etch step to produce a pattern that has a feature with a first width and sidewalls;

[[(e)]] trimming said pattern in said top photoresist and organic underlayer with a second plasma etch step to give a pattern in the bilayer stack having a feature with a second width and sidewalls, said second width is smaller than said first width; and

[[(f)]] transferring said trimmed pattern with said second width through said gate layer with a third plasma etch step to form a gate electrode.

12. (Original) The method of claim 11 wherein the gate layer is polysilicon with a thickness between about 500 and 5000 Angstroms.

13. (Original) The method of claim 11 wherein the top photoresist is a silicon containing positive tone photoresist that is patterned by exposing with 193 nm, 157 nm, or EUV radiation and developing in an aqueous base solution.

14. (Original) The method of claim 11 wherein the organic underlayer has a thickness of about 1000 to 10000 Angstroms and does not react with the top photoresist layer during the photoresist coating and patterning steps.

15. (Original) The method of claim 11 wherein said first width in said top photoresist layer is less than about 100 nm.

16. (Original) The method of claim 11 wherein the first plasma etch step comprises a 10 to 500 sccm flow rate of H2, a 10 to 500 sccm flow rate of N2, a 10 to 500 sccm flow rate of SO2, a chamber temperature of about 0° C to 100° C, a RF power from about 100 to 1000 Watts, and a chamber pressure between about 3 and 500 mTorr.

17. (Original) The method of claim 11 wherein the second plasma etch step comprises a 10 to 500 sccm Cl2 flow rate, a 1 to 50 sccm O2 flow rate, a 10 to 50 sccm HBr flow rate, a chamber temperature of about 0° C to 100° C, a RF power from about 100 to 1000 Watts, and a chamber pressure between about 3 and 500 mTorr for a period of about 5 to 200 seconds.

18. (Original) The method of claim 11 wherein the second width is more than about 10 nm smaller than the first width.

19. (Original) The method of claim 11 wherein the sidewalls formed on the organic underlayer portion of said feature are vertical or have a retrograde profile.

20. (Original) The method of claim 11 wherein the third plasma etch step comprises a 10 to 500 sccm flow rate of Cl2, a 10 to 500 sccm flow rate of HBr, a 1 to 10 sccm flow rate of O2, a chamber temperature of about 0° C to 100° C, a RF power from about 100 to 1000 Watts, and a chamber pressure between about 3 and 500 mTorr

21. (Original) The method of claim 11 wherein the third plasma etch step is performed in the same process chamber as the second plasma etch step and removes the top photoresist layer.

22. (Original) The method of claim 21 further comprised of removing the underlayer after the third plasma etch step by an oxygen ashing process.

23. (Currently Amended) A method of forming a gate electrode in a MOSFET, comprising:

[[(a)]] providing a substrate with isolation regions formed therein and with a gate stack comprised of a gate layer on a gate dielectric layer formed on said substrate between said isolation regions;

[[(b)]] forming a bilayer stack comprised of a top photoresist layer with a surface region and an organic underlayer on said gate layer, said organic underlayer is thicker than said top photoresist layer;

[[(c)]] patternwise exposing a surface region of the top photoresist layer;

[[(d)]] selectively silylating portions of the top photoresist layer to give silylated portions having a first width;

[[(e)]] forming a pattern having a feature with a first width in said top photoresist layer by a first plasma etch step that removes non-silylated portions in the surface region and the underlying top photoresist layer;

[[(f)]] transferring said pattern through the organic underlayer with a second plasma etch step, said pattern has a feature with sidewalls and a first width;

[[(g)]] trimming said pattern in said top photoresist layer and organic underlayer with a third plasma etch step to give a pattern in the bilayer stack having a feature with sidewalls and a second width, said second width is smaller than said first width;

[[(h)]] transferring said trimmed pattern with said second width through said gatelayer with a fourth plasma etch step to form a gate electrode having a second width.

24. (Original) The method of claim 23 wherein the gate layer is polysilicon with a thickness between about 500 and 5000 Angstroms.

25. (Original) The method of claim 23 wherein the top photoresist is patternwise exposed with 193 nm, 157 nm, or EUV (13 nm) wavelengths that chemically alter only the exposed surface region of said top photoresist.

26. (Original) The method of claim 23 wherein the underlayer has a thickness of about 1000 to 10000 Angstroms and does not react with the photoresist layer during the photoresist coating and patterning steps.

27. (Original) The method of claim 23 wherein the first plasma etch comprises an oxygen containing plasma.

28. (Original) The method of claim 23 wherein the second plasma etch step comprises a 10 to 500 sccm flow rate of H2, a 10 to 500 sccm flow rate of N2, a 10 to 500 sccm flow rate of SO2, a chamber temperature of about 0° C to 100° C, a RF power from about 100 to 1000 Watts, and a chamber pressure between about 3 and 500 mTorr.

29. (Original) The method of claim 23 wherein the third plasma etch step comprises a 10 to 500 sccm Cl2 flow rate, a 1 to 50 sccm O2 flow rate, a 10 to 50 sccm HBr flow rate, a chamber temperature of about 0° C to 100° C, a RF power from about 100 to 1000 Watts, and a chamber pressure between about 3 and 500 mTorr for a period of about 5 to 200 seconds.

30. (Original) The method of claim 23 wherein the second width is more than about 10 nm smaller than the first width.

31. (Original) The method of claim 23 wherein the fourth plasma etch step is performed in the same chamber as the third plasma etch step and removes the top photoresist layer.

32. (Original) The method of claim 23 wherein the fourth plasma etch step comprises a 10 to 500 sccm flow rate of Cl2, a 10 to 500 sccm flow rate of HBr, a 1 to 10 sccm flow rate of O2, a chamber temperature of about 0° C to 100° C, a RF power from about 100 to 1000 Watts, and a chamber pressure between about 3 and 500 mTorr.

33. (Original) The method of claim 23 further comprised of removing the underlayer after the fourth plasma etch step by an oxygen ashing process.

34. (Original) The method of claim 23 wherein said exposed surface regions of the top photoresist layer are selectively silylated.

35. (Original) The method of claim 23 wherein portions of the top photoresist layer between said exposed surface regions are selectively silylated.

36. (New) The method of claim 1 wherein the substrate includes isolation regions formed therein and a gate stack comprised of a gate layer on a gate dielectric layer formed on said substrate between said isolation regions.

37. (New) The method of claim 36 further comprising:

selectively silylating portions of the top photoresist layer to give silylated portions having the first width; and

wherein the step of forming a pattern includes removing non-silylated portions in the surface region and the underlying top photoresist layer